CT1836 Type A+DC6mA

RCD sensor

Version: V1.04

Overview

CT1836 is an A+6 type leakage detection magnetic ring. When combined with the ILM2112TQC chip externally, it implements a B-type residual current detection device that also complies with A+6 requirements for AC charging piles. It features digital output, high precision, low temperature drift, and high anti-interference performance. The functionality meets the requirements of IEC and GB standards for charging piles. The ILM2112TQC chip provides users with a complete solution; only simple peripheral circuits are needed to achieve high-performance leakage current detection for charging piles.

Key Features

- Digital output
- Built-in self-test function
- 5V power supply
- Low temperature drift
- Standard compatibility

Standards Compliance

- IEC 62955 – Residual direct current detecting device (RDC-DD) for permanently connected AC electric vehicle charging stations
- IEC 61851 – Electric vehicle conductive charging system
- IEC 62752 – In-cable control and protection device (IC-CPD) for Mode 2 charging of electric road vehicles
- GB/T 40820 – DC residual current detecting device (RDC-DD) for Mode 3 charging of electric vehicles
- GB/T 22794 – Type F and Type B residual current operated circuit-breakers, with or without overcurrent protection for household and similar uses

Magnetic Ring Dimensions

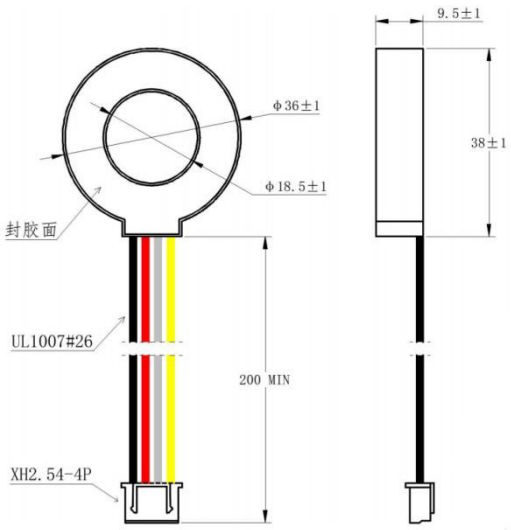


Figure 1

Magnetic Ring Pin Description

Wire Color	Function	Turns
Red	Residual current detection coil	100
Black	Residual current detection coil	100
White	Self-test coil	2
Yellow	Self-test coil	2

Magnetic Ring Electrical Parameters

No.	Function	Parameter	Unit

01	Insulation withstand voltage	No breakdown or flashover between primary and secondary windings AC 4 kV, 1 min, leakage current < 1 mA	
02	Insulation resistance	Primary to secondary windings ≥ 1000 MΩ 500 VDC	
03	Operating temperature	-40 ~ +105	℃
04	Relative humidity	≤95%	

Reference Circuit

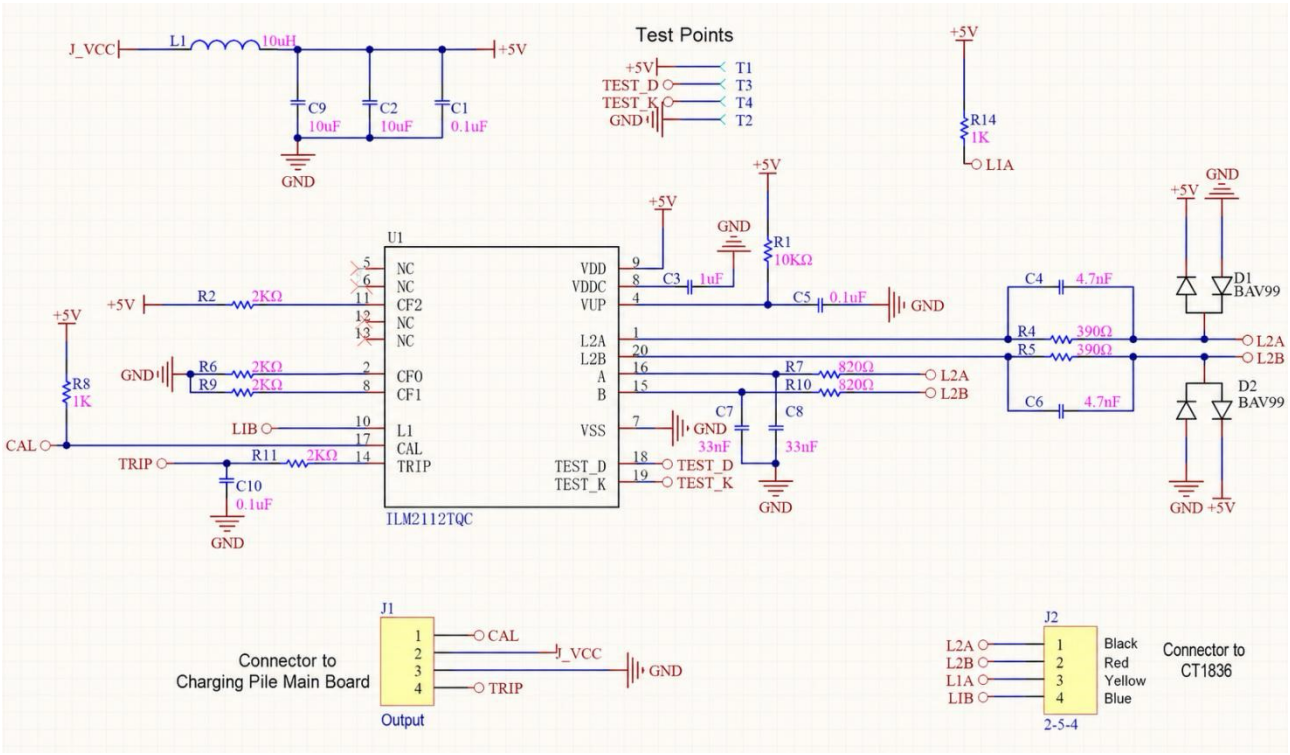
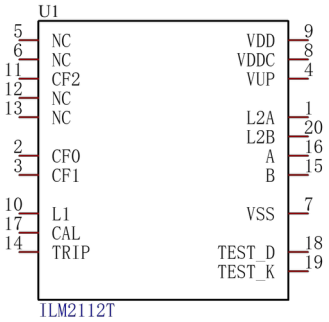


Figure 2

In the reference circuit, J1 is the interface to the charging pile main board, J2 is connected to CT1836, and U1 is the ILM2112TQC chip.

T1–T4 are test points; users should reserve these when designing the PCB.

ILM2112TQC Chip Pin Description



Pin	Pin Name	Description
1	L2A	Connected to residual current detection coil A
2	CF0	Input, configuration pin for matching CT model
3	CF1	Input, configuration pin for matching CT model
4	VUP	External RC circuit, see reference circuit
5	NC	No connection
6	NC	No connection
7	VSS	Ground
8	VDDC	Connected to 1 μF capacitor
9	VDD	5V power supply
10	L1	2-turn coil pin
11	CF2	Input, configuration pin for matching CT model
12	NC	No connection
13	NC	No connection
14	TRIP	Leakage signal output
15	B	Coil detection B
16	A	Coil detection A
17	CHK	Input, calibration pin
18	TEST_D	Reserved test pad
19	TEST_K	Reserved test pad
20	L2B	Connected to residual current detection coil B

Figure 2 shows a reference leakage ring design using CT1836 and ILM2112TQC. Connector J1 is the interface to the charging pile main board. CAL is the leakage self-test input, and TRIP is the leakage digital output signal. The timing of these two pins is described below.

Pin 17 is a 5V TTL level input. Since the charging pile MCU IO port is generally 3.3V, a transistor can be used to convert 3.3V to 5V.

CF0, CF1, and CF2 are three configuration pins. Different CT models require different logic levels, as shown below:

CT Model	CF2	CF1	CF0
CT2728	0	0	0
CT1719	1	1	1
CT1836	1	0	0

BOM:

Description	Designator	Qty
X7R 0.1 µF 25V 10% 0603	C1, C5, C10	3
X7R 10 µF 25V 10% 0603	C2, C9	2
X7R 1 µF 25V 10% 0603	C3	1
X7R 4.7 nF 50V 10% 0603	C4, C6	2
X7R 33 nF 50V 10% 0603	C7, C8	2
BAV99 100V 0.125A SOD-123	D1, D2	2
Socket with latch, straight 4PIN P2.5 CT1836	J2	1
MCL2012H100MT 0805 10 µH 0.1A	L1	1
10 kΩ 0603 1%	R1	1
2 kΩ 0603 1%	R2, R6, R9, R11	4
390 Ω 0603 1%	R4, R5	2
820 Ω 0603 1%	R7, R10	2
1 kΩ 0603 1%	R8, R14	2
ILM2112TQC TSSOP-20	U1	1

Chip Absolute Maximum Ratings

Parameter	Unit	Min	Max	Remarks
VCC	V	-0.3	6	Power supply
TA	℃	-40	85	Operating temperature
TA-S	℃	-40	105	Storage temperature

Chip Electrical Characteristics

Ta = 25℃, Vcc = 5V

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.8	5	5.2	V
Operating current	IC	-	14	-	mA
TRIP pin (output) High	VH	4.2	5	5	V
TRIP pin (output) Low	VL	0	-	0.6	V
CHK pin (input) High	VH	4.2	-	Vcc	V

CHK pin (input) Low	VL	0	-	0.5	V
Operating temperature	TA	-40	-	85	℃
Storage temperature	TA-S	-40	-	105	℃
Product weight	m	-	30	-	g
Startup time	Ton	-	-	800	ms

Residual Operating Current

Parameter	Symbol	Min	Typ	Max	Unit
DC_SM	-	3	4.5	6	mA
AC (50 Hz)	-	15	22	30	mA
A0° (50 Hz)	-	10.5	22	42	mA
A90° (50 Hz)	-	7.5	22	42	mA
A135° (50 Hz)	-	3.3	28	42	mA
2PDC	-	3.5	5.5	7	mA
3PDC	-	3.1	4.5	6.2	mA
F_ICCPD	-	15	28	42	mA

Residual Current Operating Time

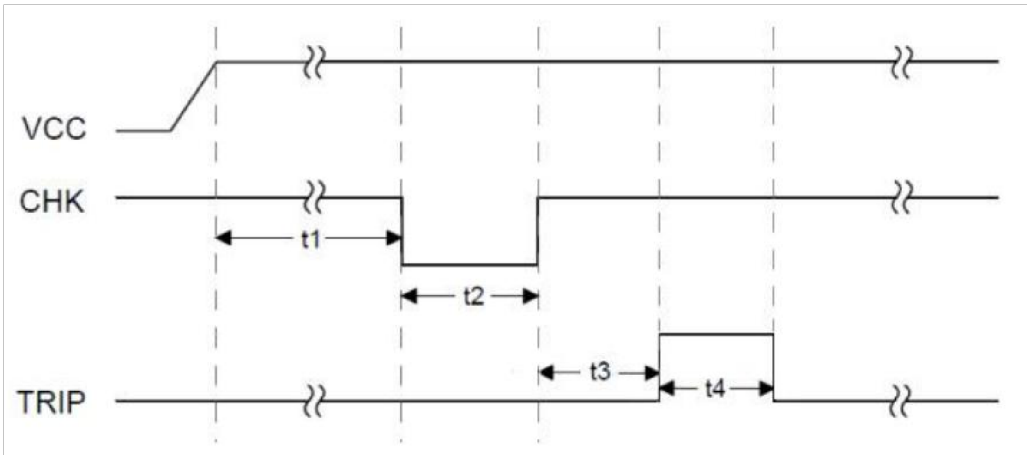
Parameter	Symbol	Min	Typ	Max	Unit
DC 6 mA	-	-	380	650	ms
DC 60 mA	-	-	63	80	ms
DC 300 mA	-	-	11	28	ms
AC 30 mA	-	-	115	200	ms
AC 60 mA	-	-	63	80	ms
AC 150 mA	-	-	15	28	ms
A0 42 mA	-	-	68	150	ms
A0 84 mA	-	-	50	100	ms
A0 350 mA	-	-	13	28	ms
A0 42 mA + 6 mA DC	-	-	73	200	ms
A0 84 mA + 6 mA DC	-	-	46	100	ms
A0 350 mA + 6 mA DC	-	-	14	28	ms
2PDC/3PDC 60 mA	-	-	63	100	ms

2PDC/3PDC 120 mA	-	-	18	80	ms
2PDC/3PDC 300 mA	-	-	12	28	ms
F_ICCPD 210 mA	-	-	15	28	ms

Instructions for Use

- Perform a self-test CHK calibration once after power-on, and again before charging.
- The chip has an 800 ms delay after power-on; during this time the chip does not respond or process anything.
- During power-on and self-test, the chip calculates the zero point.
- VCC is recommended to be generated by a 5V LDO; VCC ripple must be less than 30 mV.
- The detection magnetic ring CT1836 must be placed downstream of the charging pile switching power supply to avoid leakage current from the switching power supply Y-capacitor flowing through the magnetic ring. ● The detection magnetic ring CT1836 should be kept more than 3 cm away from relays.

Self-Test Timing

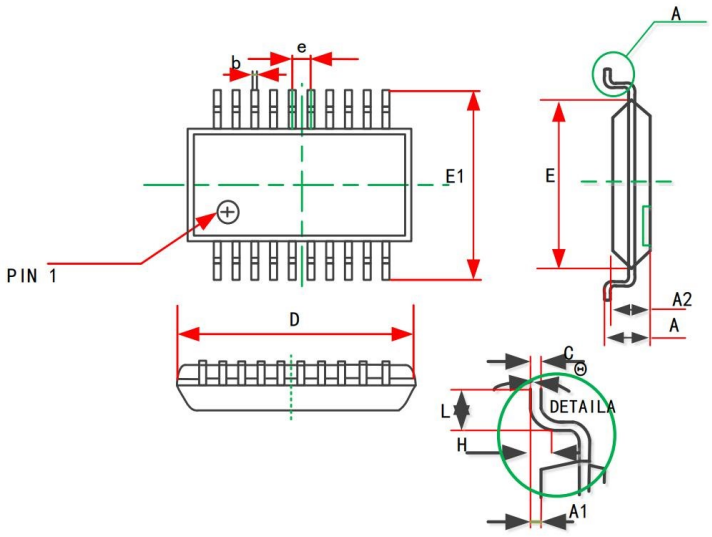


To ensure high accuracy and stable operation of the chip, the recommended parameters for t1, t2, t3, and t4 are as follows:

- t1: Waiting time after power-on completion (recommended t1 ≥ 1 s)
- t2: Time for the chip to trigger the self-test function (0.6 s ≤ t2 ≤ 1.2 s)
- t3: Waiting time for the chip to complete self-test (380 ms ≤ t3 ≤ 450 ms)
- t4: After the chip self-test passes (200 ms ≤ t4 ≤ 400 ms), the TRIP pin level flips to low, and the chip begins normal operation.

Note: During the chip self-test process, after the TRIP signal output is complete, then close the charging pile main relay.

Chip Package Information



SYMBOL	Dimensions IN Millimeters		Dimensions IN Inches	
	MIN	MAX	MIN	MAX
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	-	1.200	-	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Warranty

Product quality issues should be reported to the distributor within one year.

Any direct damage or failure caused by user negligence, misuse, installation, repair, or natural damage is not covered by the warranty.

Revision History

Version	Description	Date
V1.0	Initial release	2024.06.15
V1.01	Text corrections	2025.03.02
V1.02	Added magnetic ring description	2025.06.08
V1.03	Added C10	2025.09.05
V1.04	Removed reserved diode D3	2025.11.01